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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : **Confirmation No. 5041**  
Mitsuaki OSHIMA et al. : Docket No. 2004\_0199  
Serial No. 10/772,364 : Group Art Unit 2115  
Filed February 6, 2004 : Examiner D. Butler  
DATA PROCESSING APPARATUS : **Mail Stop: AMENDMENT**

**PATENT OFFICE FEE TRANSMITTAL FORM**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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ACCOUNT NO. 23-0975

Sir:

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Petition for Extension of Time ..... \$120.00

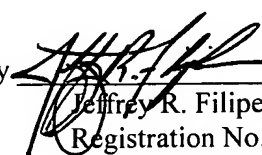
Terminal Disclaimer ..... \$110.00

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*The Commissioner is authorized to charge any deficiency or to credit any overpayment associated with this communication to Deposit Account No. 23-0975, with the EXCEPTION of deficiencies in fees for multiple dependent claims in new applications.*

Respectfully submitted,

Mitsuaki OSHIMA et al.

By  \_\_\_\_\_  
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April 15, 2005

[Check No. 67741]  
2004\_0199



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**RESPONSE**

Commissioner for Patents  
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Alexandria, VA 22313-1450

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FEES FOR THIS PAPER TO DEPOSIT  
ACCOUNT NO. 23-0975

Sir:

This paper is in response to the Office Action mailed December 15, 2004, the period for response to which having been extended by one month to April 15, 2005.

Claims 19-26 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 and 5-7 of U.S. Patent No. 6,795,929 in view of Perry.

A Terminal Disclaimer is filed concurrently herewith as a simple expedient to obviate the double patenting rejection. Accordingly, it is submitted that the double patenting rejection has been overcome.

The Terminal Disclaimer is intended simply to serve the statutory function of removing the double patenting rejection and is not meant to raise a presumption or estoppel on the merits of the double patenting rejection asserted by the Examiner.

Applicants traverse the rejection of claims 19-26 as being obvious over claims 1-3 and 5-7 U.S. Patent 6,795,929 in view of Perry for at least the following reasons.

Claim 19 recites a second processing section that has an operation state, a stop state and a power supply stop state, in the operation state the second processing section operates in accordance

with a second clock having a second frequency, in the stop state the second processing section stops operating in accordance with the second clock while the power supply to the second processing section is maintained, in the power supply stop state the power supply to the second processing section is stopped. Claim 20 recites a second processing section that has an operation state, a lower-operation state and a power supply stop state, in the operation state the second processing section operates in accordance with a second clock having a second frequency, in the lower-operation state the second processing section operates in accordance with a clock having a frequency which is lower than the second frequency while the power supply to the second processing section is maintained, in the power supply stop state the power supply to the second processing section is stopped.

Claims 1-3 of U.S. Patent 6,795,929, applied by the Examiner, recite that the second processing section has an operation state in which the second processing section operates in accordance with a second clock, and a stop state in which the second processing section stops operating in accordance with the second clock. Claims 5-7 of U.S. Patent 6,795,929 recite that the second processing section has an operation state in which the second processing section operates in accordance with a second clock, and a lower operation state in which the second processing section operates in accordance with a clock having a frequency lower than the frequency of the second clock.

The Examiner applied Perry as a secondary reference. The Examiner points out that Perry discloses the use of multiple power supply levels which are a function of the task to be performed (Perry column 2, lines 46-48), and asserts that it would therefore have been obvious to combine Perry with the invention of claims 1-3 and 5-7 of U.S. Patent 6,795,929 because of Perry's suggestion of using multiple power supply levels.

However, an obvious combination of the invention of claims 1-3 and 5-7 of U.S. Patent 6,795,929 and Perry would not yield a second processing section that has an operation state in which the processing section operates in accordance with the second clock, a stop state in which the processing section stops operating in accordance with the second clock (or the lower operation state of claim 20), and a power supply stop state in which the power supply to the processor is stopped. It is submitted that it would not have been obvious in view of the teaching of Perry to add a power

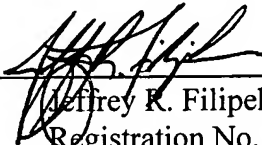
supply stop state in addition to the "stop state" of claims 1-3 of U.S. Patent 6,795,929 or in addition to the "lower operation state" of claims 5-7 of U.S. Patent 6,795,929. Accordingly it is submitted that the inventions of claims 19-26 of the present application would not result from an obvious combination of the inventions of claims 1-3 and 5-7 of U.S. Patent 6,795,929 and Perry.

At least because of the distinctions discussed above, it is submitted that the inventions recited in claims 19-26 of the present application would not have been obvious to a person having ordinary skill in the art at the time the present invention was made in view of the inventions recited in claims 1-3 and 5-7 of U.S. Patent 6,795,929 and Perry. Accordingly, it is submitted that the present application is in condition for allowance.

The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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April 15, 2005